



PONDICHERRY UNIVERSITY DEPARTMENT OF PHYSICS

Invited Lecture

on

"Spin-Orbit Torque MRAM: A solution for cache memories? "

By

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Time: 11:00 a.m.

Venue: Raman Seminar Hall, Department of Physics

All are Welcome

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Spin-Orbit Torque MRAM: A solution for cache memories?

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1. INTRODUCTION

The microelectronics industry is facing major challenges related to power dissipation and energy consumption with both static and dynamic consumption limiting microprocessor performance growth. Multicore processors whereupon a fraction of the cores are active at any given time is only a stopgap hiding the soon to come power wall. A real breakthrough could come from integrating nonvolatility in on-chip memory, which represents today more then 70% of the total silicon area. For this to happen, a new class of electrically addressable, nonvolatile is required. In current multicore architectures, three levels of cache memories coexist, with different sizes and performance ranging from L1 cache with KB capacity and ~ns access time to L3 cache with multi-MB capacities and ~70ns access time. Cache memories typically use Static Random Access Memory (SRAM) technology, which is much faster than DRAM at the expense of higher cost (e.g. silicon area). Multiple candidates exist, however none fulfills the combined requirements for high speed, low active power and infinite endurance. Spin Transfer Torque Magnetic Random Access Memory (STT-MRAM) has been identified by the ITRS as the most credible candidate, yet its practical (e.g. product-compatible) operation speed is still too low to act as L1 cache.

Spin-Orbit Torque (SOT) MRAM is an alternative technology which concept has been proposed only very recently [1]. In SOT MRAM, a current flowing in the plane of a magnetic multilayer exhibiting a strong structural inversion asymmetry exerts a spin-orbit coupling-induced torque on the magnetization, which can lead to magnetization reversal in multiple configurations, including perpendicular magnetic layers. The key advantage of the SOT-MRAM is that the writing sequence does not involve anymore a current flowing through the MRAM cell itself, therein naturally solving any reliability issues of current STT-MRAM. Furthermore, having independent read and write paths allows for a greater flexibility in material parameters optimization, in particular to achieve maximum

magnetoresistance (e.g. large read speed) whilst keeping a low writing current (e.g. active power).

The first proof of concept of a bit-cell consisting of a full magnetic tunnel junction (MTJ) with perpendicular magnetization and an SOT-driven storage layer has been demonstrated using state-of-the-art FeCoB/MgO/CoFeB stack [2]. The basic write (e.g. magnetization switching by SOT) and read (e.g. TMR signal detection) operations have been demonstrated in magnetic dots with dimensions down to 100nm and with current pulse width of 50ns.

We then show that deterministic bipolar switching can be achieved down to 180ns pulses without evidence for precessional switching behavior. The dependence of the critical current I_c on pulse width τ_p shows that I_c scales linearly with $1/\tau_p$, from very short pulse width up to ms [3]. Micromagnetic simulations show that the reversal process is governed by a nucleation / propagation process, with domain nucleation at the edge of the dot.

While initial studies were focused on Pt/Co/AlOx [1], the focus quickly shifted towards Ta/CoFeB/MgO, due to the higher spin-orbit coupling of Ta and the readily achievable perpendicular magnetic anisotropy (PMA) and larger TMR in such systems [4]. Alternative materials may also be considered, such as W for which a giant spin Hall effect is reported [5]. Promising results are obtained in W/Hf/CoFeB/MgO MTJs with PMA and 80% TMR.

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- [5] [4] C.-F. Pai et al. Appl. Phys. Lett. 101, 122404 (2012)