
**PONDICHERRY UNIVERSITY**
**PUDUCHERRY 605 014**
**Department of Electronics Engineering**

# M. Tech Electronics

## Scheme & Syllabus

## 2010-11 Onwards

# M.Tech. Program in Electronics

Department of Physics will mentor the **M.Tech. Program in Electronics**, which is to be introduced from the academic year 2010-11.

Electronics plays important role in the development of the state of the art science and technology. Advancement of Electronics led to an all round development on human comfort, safety and furthers research on almost all scientific technology and engineering endeavours. M. Tech. (Electronics) program is envisaged as a science, engineering and technology.

M. Tech. program is designed to impart the necessary background knowledge of the state of art developments in all the areas of electronics – devices to systems. The modern physics courses in most of the universities at graduate and post - graduate level of science try to cover the fundamental aspects of electronics Viz., semi-conductor physics and circuit theory. The engineering graduates are specialized only in technological aspects of the application of theses devices and circuits in instrumentation and communication systems. The present M.Tech. program is aimed to bridge this gap between the science and technology students. The emphasis will be on understanding both the science and technological aspects of electronics. Further it will enable them to design new devices and systems.

The program is planned to cover the following aspects in detail.

1. Devices: Design, fabrication and Application
2. Communication: Microwave, digital and optical communication
3. System design: Analog, digital and mixed-mode.
4. Embedded Systems: Real time and Robotics applications

The students who pass out of this course will have good Industrial and research opportunities.

## Details of the program

**Program Duration:**
Two years (Four Semesters); Total number of credits: 73

**Eligibility criteria:**
B.E /B.Tech in EEE, ECE and E&I , M.Sc. Electronic Science / Physics with Electronics/ Materials Science with Electronics / Solid State Technology with Electronics

**Admission criteria:**
Pondicherry University – All India Entrance Examination
Or valid GATE Score in relevant disciplines
**Intake:** 25 students

**Teaching and Learning Methods:**
Lectures, tutorials and seminars form the main methods of course delivery enhanced by individual and group project work, laboratory work, computing workshops and industrial visits.

**Assessment Methods:**
Assessment will be through Chaise Based Credit System (CBCS) through session (laboratory reports, class tests, set assignments) or by continuous assessment (designing, computer practical, seminar papers, project reports etc.) and end semester examinations. The end semester question paper can be set by concerned course teacher

**Scheme of Courses and Credits for M.Tech Electronics:**

| **First year**: | **Odd semester** | **Even Semester** |
|---|---|---|
| Compulsory subjects | 3 | 3 |
| Elective Subjects | 2 | 3 |
| Practical – Laboratory | 1 | 1 |
| **Second year** | | |
| Project work & Dissertation | 1 | 1 |

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Centre Head
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Department of Physics, Pondicherry University

## Scheme of Study

| S.No | Course No. | Course Title. | L-T-P | Credits |
|---|---|---|---|---|
| **SEMESTER- I** | | | | |
| 1. | EEC7100 | Advanced Electronic Design Laboratory | 0-0-6 | 2 |
| 2. | EEC7101 | Applied Mathematics | 3-1-0 | 4 |
| 3. | EEC7102 | Semiconductor devices & Technology | 3-1-0 | 4 |
| 4. | EEC7103 | Digital Signal Processing | 3-1-0 | 4 |
| 5. | EEC7104 | Elective - I | 2-1-0 | 3 |
| 6. | EEC7105 | Elective – II | 2-1-0 | 3 |
| | | | | **20** |
| **List of Electives – I & II** | | | | |
| 7. | EEC7104 | Microcontrollers & Embedded systems | 2-1-0 | |
| 8. | EEC7105 | Nanoelectronics | 2-1-0 | |
| 9. | EEC7106 | Electromagnetic Theory, Interference & Compatibility | 2-1-0 | |
| 10. | EEC7107 | Institute PG course | 2-1-0 | |
| **SEMESTER – II** | | | | |
| 11. | EEC7200 | Advanced Embedded Systems laboratory | 0-0-6 | 2 |
| 12. | EEC7201 | Micro-electromechanical systems, MEMS | 3-1-0 | 4 |
| 13. | EEC7202 | Analog & Digital Design Techniques | 3-1-0 | 4 |
| 14. | EEC7203 | Research Seminar | 1-0-0 | 2 |
| 15. | | Elective – III | 2-1-0 | 3 |
| 16. | | Elective – IV | 2-1-0 | 3 |
| 17. | | Elective – V | 2-1-0 | 3 |
| | | | | **21** |
| | | | | |

| | | | | |
|---|---|---|---|---|
| **S.No** | **Course No.** | **Course Title.** | **L-T-P** | **Credits** |
| **List of Electives – III, IV & V** | | | | |
| **Group-A: VLSI Technology** | | | | |
| 18. | EEC7204 | VLSI Technology | 2-1-0 | |
| 19. | EEC7205 | VLSI Systems & Architecture | 2-1-0 | |
| 20. | EEC7206 | CAD Tools for VLSI Design | 2-1-0 | |
| 21. | EEC7207 | CMOS VLSI Design | 2-1-0 | |
| 22. | EEC7208 | ASIC Design | 2-1-0 | |
| 23. | EEC7209 | Low Power VLSI Design | 2-1-0 | |
| 24. | EEC7210 | Design Analog & Mixedmode VLSI Circuits | 2-1-0 | |
| 25. | EEC7211 | Alogarithm for VLSI | 2-1-0 | |
| 26 | EEC7212 | Testing & Verification | 2-1-0 | |
| **Group B: Communication Electronics** | | | | |
| 27. | EEC7213 | Passive Microwave Devices & Circuits | 2-1-0 | |
| 28. | EEC7214 | Antenna Theory & Design | 2-1-0 | |
| 29. | EEC7215 | Optical Communication & Networking | 2-1-0 | |
| 30. | EEC7216 | Wireless communications | 2-1-0 | |
| 31. | EEC7217 | Advanced Digital Communications | 2-1-0 | |
| 32. | EEC7218 | Active RF & Microwave Circuits | 2-1-0 | |
| 33. | EEC7219 | CMOS RF Circuit Design | 2-1-0 | |
| 34. | EEC7220 | Modelling & Simulation of Networks | 2-1-0 | |
| **SEMESTER – III & IV** | | | | |
| 35. | EEC7300 | Phase I – Project, Mid- Project Report – Problem Definition, Litterature Review, Preliminary results, if any & Viva voce | | **12** |
| 36. | EEC7400 | Phase-II – Project, Comprehensive Project report with results & Viva Voce | | **20** |
| **TOTAL NUMBER OF CREDITS TO BE OBTAINED FOR THE COURSE** | | | | **73** |

## EEC7100 Advanced Electronic Design Laboratory 0-0-2 Credits 2

***Following is the list of suggested components for this lab***

1. Electronics Design Lab - Analog and Digital circuits design, evaluation, experimental
2. Power Electronics Lab – Power converters, controllers design & evaluation facility
3. Instrumentation Lab – Sensors, signal conditioners, display & testing facilities
4. Microwave Lab – Microwave generation, communication and reception & test facilities

## EEC7101 Advanced Engineering Mathematics 4-0-0 Credits 4

**Unit-I** **10 hours**

**Vector Calculus :** Vector and Scalar Functions and Fields; Gradient and Directional Derivative of Scalar Fields ; Divergence and Curl of Vector Fields ; Line Integrals, Path-independence properties ; Multiple Integrals, Change of variables, Jacobian ; Green's Theorem ; parametric representation of Surfaces, Tangent plane and Normal ; Surface Integrals ; Volume Integrals ; Gauss' Divergence Theorem ; Stoke's Theorem

**Unit- II** **10 hours**

**Fundamentals of matrices**, eigenvalues, eigenfunctions, adjoints, inverse etc sparse matrices; diagonal dominance; non-positive and non-negative matrices; positivity theorems; large set of simultaneous equations.

**Unit- III** **15 hours**

**Ordinary Differential Equations** : Classification of Differential Equations and their role as a system modeling and analysis tool - Separable ODEs, Linear ODEs; Homogeneous vs. Non-homogeneous ODEs; Homogeneous Linear ODEs with Constant Coefficients; Method of Undetermined Coefficients ; Solution by Variation of Parameters ; Applications- Power Series Method ; Modelling and applications in different engineering problems including Electronics and mechanical problems.

**Partial differential equations** – First order partial differential equations, complete integral and general solution, methods of solution of a first and second order partial differential equation, Laplace's equation, wave equation, diffusion equations.

**Unit- IV** **10 hours**

**Integral Transforms**. Fourier, Laplace Transforms and the inverse transforms, connection to physical problems Other transforms such as Mellin and Hankel transforms, and transforms generated by Green's function. Applications for obtaining solution of ordinary/partial differential equations.

**Unit – IV Probability and Statistics:** **10 hours**

Probability Spaces- Discrete probability distributions, Continuous probability densities . Distribution functions, Multiple random variables and joint distributions. Expectations, moments, Characteristic functions and moments generating functions, Poisson processes – Exponential distribution and applications; Birth-death processes and applications. Law of large numbers – Central limit theorem.

TEXT BOOKS


1. E. Butkov , Mathematical Physics, Addison-Wesley, 1973.
2. W.Lauterborn, T.Kurz, M.Wiesenfeldt, Coherent Optics and Applications , Springer, 1995.
3. K Kreyszig , Advanced Eng. Mathematics , Seventh Edition, John Wiley &Sons,1995 .
4. Mathematical Methods for Physicists, G. B. Arfkin and H. J. Weber.
5. Elements of Partial Differential Equations, I. Sneddon
6. Hole, P.G., Port, S.C., and Stone,C.J.,' Introduction to Probability Theory', Indian Edition Universal Book Stall, New Delhi,1998.
7. M. Remoisenet , *Waves called Solitons: Concepts and Experiments*-, Springer Verlag, 1992

## EEC7102 Electronic Devices & Technology 4-0-0 Credits4

**UNIT – I** **15 hours**

**Semiconductor Physics:** Review of crystal structure, Crystal structure of important semiconductors (Si, Ge & GaAs), Review of quantum mechanics, Electrons in periodic lattices, E-k diagrams, Quasiparticles in semiconductors, electrons, holes and phonons. Carrier concentration and carrier transport phenomenon. Excess carriers in semiconductors: Doping, Injection and recombination mechanisms; Carrier statistics; Continuity equation, Poisson's equation and their solution; Optical, Thermal and High field properties of semiconductors.

**UNIT – II** **10 hours**

**Semiconductor junctions:** Schottky, Homo- and Hetero-Junctions: Band diagrams, I-V and C-V characteristics (Analytical expressions); Small signal switching models; Two terminal and surface states devices based on semiconductor junctions. Transistors (BJT & JFET): Band diagrams, I-V and C-V characteristics (Analytical expressions).

**UNIT – III** **15 hours**

**MOS structures:** Semiconductor surfaces; The ideal and non-ideal MOS capacitor band diagrams and CVs; Effects of oxide charges, defects and interface states; passivation of interface states; Characterization of MOS capacitors: HF and LF CVs, avalanche injection; High field effects and breakdown. MOSFET and CCD: Band diagrams, I-V and C-V characteristics (Analytical expressions); Scaling down and quantum tunneling effects; Alternate high k-dielectric materials; Hf-MOSFETs.

**UNIT – IV** **15 hours**

**Fabrication and Characterization Techniques:** Crystal growth and wafer preparation, Formation of p-n junction, Thinfilm deposition and oxidization techniques, Planar technology: Masking and lithography techniques, e-beam and other advanced lithography techniques. Bipolar and MOS integration techniques. Interface passivation techniques. Characterization techniques: Four-probe and Hall measurement; I-V and CVs for dopant profile characterization; Capacitance transients and DLTS.

**TEXT BOOKS:**


1. S. M. Sze, Physics of Semiconductor Devices, 2nd edition John Wiley, 1981.
2. J. P. McKelvey, Introduction to Solid State and Semiconductor Physics, Harper and Row and John Weathe Hill.
3. M.S. Tyagi, Introduction to Semiconductor Materials and Devices, John Wiley & Sons, 1991.


**REFERENCE BOOKS**


4. J. Singh, Semiconductor devices: Basic Principles, Wiley student edition 2004

## EEC7103 Digital Signal Processing 4-0-0 Credits 4

**Unit-I** **15 hours**

Digital Signal Processing Fundamentals: Review of DSP Fundamentals ; FIR filter design by windowing; Adaptive filtering techniques; Fourier analysis of signal using FFT; : Introduction to Real time DSP Discrete Time Signals: Sequences, representation of signals on orthogonal basis, Sampling and Reconstruction of signals.

**Unit-II** **15 hours**

Discrete Systems: Attributes, Z-Transform, Analysis of LTI systems, Frequency Analysis, Inverse Systems, Discrete Fourier Transform (DFT), Fast Fourier Transform algorithm, Implementation of Discrete Time Systems.

**Unit-III** **15 hours**

Design of FIR Digital Filters: Window method, Park-McClellan's method.
Design of IIR Digital Filters: Butterworth, Chebyshev and Elliptic Approximations; Lowpass, Bandpass, Bandstop and High pass filters. Effect of finite register length in FIR filter design. Parametric and non-parametric spectral estimation. Introduction to multirate signal processing.

**Unit- IV** **15 hours**

Application of DSP to Speech and Radar signal processing.
Implementaion of DSP Systems : Motorola DS5630X, Architecture,; Instruction set; Addressing modes; Simple 5630X program; Real time digital FIR filter; Real time LMS adoptive filers; Real time frequency domain processing

TEXT BOOKS:


1. A.V. Oppenheim and Schafer, “Discrete Time Signal Processing”, Prentice Hall, 1989.
2. John G. Proakis and D.G. Manolakis, “Digital Signal Processing: Principle”, Algorithms and Applications, Prentice Hall, 1997.
3. L.R. Rabiner and B. Gold, “Theory and Application of Digital Signal Processing”, Prentice Hall, 1992.
4. J.R. Johnson, “Introduction to Digital Signal Processing”, Prentice Hall, 1992.
5. D. J. DeFatta, J. G. Lucas and W. S. Hodgkiss, “Digital Signal Processing”, J Wiley and Sons, Singapore, 1988.

## EEC7104 Microcontrollers & Embedded systems 3-0-0 Credits 3

**Unit-I: INTRODUCTION TO EMBEDDED SYSTEMS** **8 hours**

Definition and Classification – Overview of Processors and hardware units in an embedded system – Software embedded into the system – Exemplary Embedded Systems – Embedded Systems on a Chip (SoC) and the use of VLSI designed circuits

**Unit-II: DEVICES AND BUSES FOR DEVICES NETWORK** **10 hours**

I/O Devices - Device I/O Types and Examples – Synchronous - Iso-synchronous and Asynchronous Communications from Serial Devices - Examples of Internal Serial-Communication Devices - UART and HDLC - Parallel Port Devices - Sophisticated interfacing features in Devices/Ports- Timer and Counting Devices - '12C', 'USB', 'CAN' and advanced I/O Serial high speed buses- ISA, PCI, PCI-X, cPCI and advanced buses.

**Unit-III: PROGRAMMING CONCEPTS AND EMBEDDED PROGRAMMING IN C, C++** **8 hours**

Programming in assembly language (ALP) vs. High Level Language - C Program Elements, Macros and functions -Use of Pointers - NULL Pointers - Use of Function Calls – Multiple function calls in a Cyclic Order in the Main Function Pointers – Function Queues and Interrupt Service Routines Queues Pointers – Concepts of EMBEDDED PROGRAMMING in C++ - Objected Oriented Programming – Embedded Programming in C++, 'C' Program compilers – Cross compiler – Optimization of memory codes.

**UNIT- IV: REAL TIME OPERATING SYSTEMS – PART - 1** **12 hours**

Definitions of process, tasks and threads – Clear cut distinction between functions – ISRs and tasks by their characteristics – Operating System Services- Goals – Structures- Kernel - Process Management – Memory Management – Device Management – File System Organisation and Implementation – I/O Subsystems – Interrupt Routines Handling in RTOS, REAL TIME OPERATING SYSTEMS : RTOS Task scheduling models - Handling of task scheduling and latency and deadlines as performance metrics – Co-operative Round Robin Scheduling – Cyclic Scheduling with Time Slicing (Rate Monotonics Co-operative Scheduling) – Preemptive Scheduling Model strategy by a Scheduler – Critical Section Service by a Preemptive Scheduler – Fixed (Static) Real time scheduling of tasks - INTER PROCESS COMMUNICATION AND SYNCHRONISATION – Shared data problem – Use of Semaphore(s) – Priority Inversion Problem and Deadlock Situations – Inter Process Communications using Signals – Semaphore Flag or mutex as Resource key – Message Queues – Mailboxes – Pipes – Virtual (Logical) Sockets – Remote Procedure Calls (RPCs).

**Unit-V: REAL TIME OPERATING SYSTEMS – PART – 2** **10 hours**

Study of Micro C/OS-II or Vx Works or Any other popular RTOS – RTOS System Level Functions – Task Service Functions – Time Delay Functions – Memory Allocation Related Functions – Semaphore Related Functions – Mailbox Related Functions – Queue Related Functions – Case Studies of Programming with RTOS – Understanding Case Definition – Multiple Tasks and their functions – Creating a list of tasks – Functions and IPCs – Exemplary Coding Steps.

**TEXTBOOKS**:1. Rajkamal, Embedded Systems Architecture, Programming and Design, TATA McGraw-Hill, First reprint Oct. 2000

**REFERENCES:** 1. Steve Heath, Embedded Systems Design, Second Edition-2003, Newnes,

2. David E.Simon, An Embedded Software Primer, Pearson Education Asia, First Indian Reprint 2000.
3. Wayne Wolf, Computers as Components; Principles of Embedded Computing System Design – Harcourt India, Morgan Kaufman Publishers, First Indian Reprint 2001
4. Frank Vahid and Tony Givargis, Embedded Systems Design – A unified Hardware /Software Introduction, John Wiley, 2002.

## EEC7105 Nanoelectronics 3-0-0 Credits 3

**Unit-I** **12 hours**

Introduction to nano-science, review of quantum confinement theory, quantum size effects: electrical, mechanical and optical properties, low dimensional systems (quantum well, quantum wire and quantum dots). Quantum tunneling effects in electronic devices.

**Unit-II** **12 hours**

Shrink-down Approaches: Introduction, CMOS Scaling, The nanoscale MOSFET, Finfets, Vertical MOSFETs, limits to scaling, system integration limits (interconnect issues etc.), Resonant Tunneling Transistors, Single electron transistors, new storage, optoelectronic, and spintronics devices.

**Unit-II** **12 hours**

Atoms-up Approaches: Molecular electronics involving single molecules as electronic devices, transport in molecular structures, molecular systems as alternatives to conventional electronics, molecular interconnects;

**Unit-IV** **10 hours**

Carbon nanotube electronics, band structure & transport, devices, applications.

TEXT BOOKS:

1. C.P. Poole Jr., F.J. Owens, “Introduction to Nanotechnology”, Wiley (2003).
2. Waser Ranier, “Nanoelectronics and Information Technology” (Advanced Electronic Materials and Novel Devices), Wiley-VCH (2003)
3. K.E. Drexler, “Nano systems”, Wiley (1992)
4. K.Goser, P. Golsekotter, J. Dienstuhl, “Nanoelectronics and Nanosystems: from transistors to molecular and quantum devices”, Springer, 2005
5. M. Dragoman and D.Dragoman, “Nanoelectrincs-princeiples and devices” Artech house Publishers, 2005
6. M. Lunstrom, J.Guo, “Nanoscale transistors –Device physics, Modelling and Simulation”, Spriner 2005.
7. D. Goldhaber-Gordon et al, “Overview of nanoelectronic devices” Proc. Of IEEE Vol 85 No.4 Aprill 1997.

REFERENCE BOOKS:

4. John H. Davies, “The Physics of Low-Dimensional Semiconductors”, Cambridge University Press, 1998 Research Papers
5. Y.Taur and T.H. Ning, “Fundamentals of Modern VLSI devices, Cambridge Univesity Press, 1998.

## EEC7106 E.M.Theory, Interference & Compatability 3-0-0 Credits 3

**UNIT – I** **9 hours**

Maxwell's equations – Vector and scalar potentials – Gauge transformations – Lorentz and Coulomb gauges – Poynting theorem – Plane electromagnetic waves – Reflection and refraction of electromagnetic waves at an interface between dielectric and vacuum – Waves in conducting medium – Wave propagation through conductor-dielectric interface.

**UNIT – II** **12 hours**

Transmission lines – Parallel plate transmission lines – Helmoltz equation – RLCG parameters – Smith chart and its applications - Propagation constant and characteristic impedance of a general, lossless and distortionless transmission line – Quarter wavelength and half wavelength lines – Skin effect and resistance – Derivation of skin depth – Problems solving.

Retarded and advanced potentials – Lienard-Wiechert potentials – The fields of a moving point charge – Dipole radiation – Magnetic dipole radiation – radiation zone – Radiation from an arbitrary source – Larmor formula for power of radiation – Physical basis for antenna radiation.

**UNIT – III** **12 hours**

EMI Environment – Sources of EMI, conducted and radiated EMI, Transient EMI, EMI-EMC definitions, units, parameters. EMI coupling principles-Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near field cable to cable coupling. Power mains and power supply coupling.

**UNIT – IV** **12 hours**

EMI specifications, standards, limits - units of specifications, Civilian and Military standards. EMI measurements – EMI test instruments, systems, EMI test, EMI shielded chamber, Open area test site, TEM cell Antennas, conductors, sensors, injectors, couplers, Military test methods and procedures, calibration procedures.

EMI control techniques – shielding, filtering, grounding, bonding, Transient suppressors, Isolation transformer, Cable routing, signal control, component selection and mounting. EMC design of PCB – PCB traces cross talk, impedance control, power distribution decoupling, zoning, motherboard designs.

TEXT BOOKS


1. Bernhard Keiser, *Principles of Electromagnetic Compatibility,* Artech house, 3rd Edn, 1986.
2. Henry W. Ott, *Noise reduction Techniques in Electronics Systems,* John Wiley & Sons, 1988.
3. David Jackson. Classical Electrodynamics. John Wiley.
4. Mathew N Sadiku. Elements of electromagnetics. Oxford University Press.


REFERECE BOOKS


1. B Thide. Electromagnetic field theory. Upsilon books.
2. Noise Reduction Techniques in Electronic Systems, 2nd Edition - Ott HW, 1985
3. Electrostatic Damage in Electronics : Devices and Systems - Willium B Greason, Johan Wiley and Son', 1986.
4. Digital Bus Hand Book - Joseph Di Giacomo, McGraw-Hill Publishing Company, 1990.

## EEC7200 Advanced Embedded Systems laboratory 0-0-2 Credits 2

***Following is the list of suggested components for this lab***

1. Embedded system Lab – Microcontrollers, embedded system developmental facilities
2. DSP Lab – Applications of DSP –design, evaluation and testing facilities
3. Computation / Simulation lab – Modeling of devices, simulation of circuits facility
4. Communications Lab – Analog , Digital & optical communication facilities

## EEC7201 Micro-electromechanical systems 4-0-0 Credits 4

**Unit-I** **15 hours**

History of MicroElectroMechanical Systems (MEMS), market for MEMS, basics of microtechnology, lithography and etching techniques, principles of bulk and surface micromachining: subtractive processes, additive processes (evaporation, sputtering, epitaxial growth). Fundamental devices and processes,

**Unit-II** **15 hours**

Multi User MEMS Process (MUMPs), SUMMiT: design rules; applications; micro hinges and deployment actuators, CMOS MEMS, cleanroom lab techniques, MicroOptoElectroMechanical Systems (MOEMS), bioMEMS and biomaterials, piezoresistivity; scanning probe microscopy, scaling laws, applications. Lumped element modeling and design,

**Unit-III** **15 hours**

Electrostatic Actuators , Electromagnetic Actuators, Linear and nonlinear system dynamics, resonant systems, Elasticity (stress, strain, material properties), Mechanical structure basics (bending of beams, torsion, natural frequency),

**Unit-IV** **15 hours**

Optical system design basics (Gaussian beam optics, matrix optics, resolution) Application case studies: MEMS Scanners and Retinal Scanning Displays (RSD), Grating Light Valve (GLV), Digital Micromirror Devices (DMD), Optical switching, Capacitive Micromachined Ultrasonic Transducers (CMUT)

TEXT BOOKS


1. Gregory T A 1998, Kovacs Micromachined Transducers Sourcebook, WCB McGraw-Hill.
2. Nadim Maluf, An introduction to Microelectromechanical system design, Artech House, 2000
3 Victor M. Bright, Editor, Selected papers on Optical MEMS, SPIE Milestone Series, Volume MS 153, SPIE Press, 1999
4 Mohamed Gad-el-Hak, Editor, The MEMS Handbook, CRC Press, Baco Raton, 2001.
1. Marc Madou, Fundamentals of Microfabrication, CRC Press, New York, 1997


REFERENCE BOOKS.


2. Gregory T. A. Kovacs, Micromachined Transducers Sourcebook, WCB McGraw-Hill
7 W. Trimmer, Editor, Micromechanics and MEMS: Classic and Seminar Papers to 1990, IEEE Press, 1996

## EEC7202 Analog & Digital Design Techniques 4-0-0 Credits 4

**Unit-I** **8 hours**

Threshold Logic: Introductory Concepts, Synthesis of Threshold Networks.

**Unit-II** **20 hours**

Reliable Design and Fault Diagnosis Hazards: Fault Detection in Combinational Circuits, Fault-Location Experiments, Boolean Differences, Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure-Tolerant Design, Quadded Logic Capabilities, Minimization, and Transformation of Sequential Machines: The Finite-State Model, Further Definitions, Capabilities and Limitations of Finite – State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines.

**Unit-III** **15 hours**

Structure of Sequential Machines: Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, Decompositions, Synthesis of Multiple Machines.

**Unit-IV** **15 hours**

State—Identifications and Fault-Detection Experiments: Homing Experiments, Distinguishing Experiments, Machine Identification, Fault-Detection Experiments, Design of Diagnosable Machines, Second Algorithm for the Design of Fault Detection Experiments, Fault-Detection Experiments for Machines which have no Distinguishing Sequences.

TEXT BOOKS:

1. Zvi Kohavi, “Switching and Finite Automata Theory”, 2nd Edition. Tata McGraw Hill Edition
2. Charles Roth Jr., “Digital Circuits and logic Design”,
3. Parag K Lala, “Fault Tolerant and Fault Testable Hardware Design”, Prentice Hall Inc. 1985
4. E. V. Krishnamurthy, “Introductory Theory of Computer”, Macmillan Press Ltd, 1983

Refrence book:

5. Mishra & Chandrasekaran, “Theory of Computer Science – Automata, Languages and Computation”, 2nd Edition, PHI,2004

**EEC7204 VLSI TECHNOLOGY 3-0-0 Credits: 3**

**Unit-I** **15 hours**

Environment for VLSI Technology: Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques.

Impurity Incorporation: Solid State diffusion modeling and technology; Ion Implantation modeling, technology and damage annealing; characterization of Impurity profiles.

**Unit-II** **10 hours**

Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultra thin films. Oxidation technologies in VLSI and ULSI; Characterization of oxide films; High k and low k dielectrics for ULSI.

Lithography: Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation.

**Unit-III** **10 hours**

Chemical Vapour Deposition Techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modeling and technology.

Metal Film Deposition: Evaporation and sputtering techniques. Failure mechanisms in metal interconnects; Multi-level metallization schemes.

**Unit-IV** **10 hours**

Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI.

Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technologies

TEXT BOOKS:

1. C.Y. Chang and S.M.Sze (Ed), “ULSI Technology”, McGraw Hill Companies Inc, 1996.
2. Stephena, Campbell, “The Science and Engineering of Microelectronic Fabrication”, Second Edition, Oxford University Press, 2005.
3. Yuan Taur, Tak. H. Ning, “Fundamentals of Modern VLSI Devices”, Cambridge University Press, 2003
4. S.K. Gandhi, “VLSI Fabrication Principles”, John Wiley Inc., New York, 1983.

**EEC7205 VLSI SYSTEM AND ARCHITECTURE 3-0-0 Credits 3**

**Unit-I** **9 hours**

Behavior and Architecture: Dedicated and Programmable VLSI architectures, Instruction sets and through enhancement techniques (Parallelism. pipelining. cache, etc.)

**Unit-II** **12 hours**

CISC Architecture Concepts: Typical CISC instruction set and its VLSI implementation, RT-level optimization through hardware flow charting, Design of the execution unit, Design of the control part (micro programmed and hardwired), handling exceptions: Instruction boundary interrupts, immediate interrupts and traps.

**Unit-III** **12 hours**

RISC Architecture Concepts: Typical RISC instruction set and its VLSI implementation, Execution pipeline, Benefits and problems of pipelined execution, Hazards of various types of pipeline stalling, concepts of scheduling (Static and dynamic) and forwarding to reduce / minimize pipeline stalls Exceptions in pipelined processors

**Unit-IV** **12 hours**

DSP Architecture Concepts: Typical DSP instruction set and its VLSI implementation

Dedicated Hardware Architecture Concepts: Example and Case studies.
Dedicated DSP architecture Concepts: Synthesis, Scheduling and Resource allocation, Conventional Residue number, distributed arithmetic architecture

REFERENCE BOOKS:


1. D A Patterson and I L Hennessy, "Computer Architecture: A Quantitative approach", Second edition, Margon Kaufmann, 1996
2. Lars Wanhammar, "DSP Integrated Circuits", Academic Press 1999.
3. D A Patterson and J L Hennessy, "Computer organization and Design: Hardware/Software interface" Second Edition, Margan Kaufmann, 1998
4. Avtar Sing and Srinivas S, "DSP: Architecture, Programming and Applications", Thomson Learning, 2004.
5. B. Venkataramani and M. Baskar, "DSP: Architecture, Programming and Applications", TMH, 2002.

**EEC7206 CAD TOOLS FOR VLSI DESIGN 3-0-0 Credits 3**

**Unit-I** **10 hours**

High level Synthesis, CDFG representation, Partitioning algorithms, Scheduling algorithms, allocation algorithms

Logic synthesis & verification: Introduction to combinational logic synthesis, Binary Decision Diagram, Cube representation, Kernels & co-Kernals, two level synthesis, PLA PLA folding, ROBDD, ITE graphs, Sequential synthesis

**Unit-II** **14 hours**

VLSI automation Algorithms: Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms

Placement, floor planning & pin assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment

**Unit-III** **14 hours**

Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches

Detailed routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms

Over the cell routing & via minimization: two layers over the cell routers, constrained & unconstrained via minimization

**Unit-IV** **7 hours**

Compaction: problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction

TEXT BOOKS:


1. Naveed Shervani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publisher, Second edition.
2. Deniel Gajski, Nikil Dutt and Allen Wu "High Level Synthesis", Kluwer Academic
3. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.
4. Rolf Drechsheler : "Evolutionary Algorithm for VLSI", Second edition
5. Trimburger, "Introduction to CAD for VLSI", Kluwer Academic Publisher, 2002

## EEC7207 CMOS VLSI DESIGN 3-0-0 Credits:3

**Unit-I** **10 hours**

**MOS Transistor Theory:** n MOS / p MOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation. Mobility variation, tunneling, punch through, hot electron effect MOS models, small signal AC Characteristics, CMOS inverter, βn / βp ratio, noise margin, static load MOS inverters, differential inverter, transmission gate, tristate inverter, BiCMOS inverter

**Unit-II** **10 hours**

**CMOS Process Technology:** Lambda Based Design rules, scaling factor, semiconductor Technology overview, basic CMOS technology, p well / n well / twin well process. Current CMOS enhancement (oxide isolation, LDD. refractory gate, multilayer inter connect) , Circuit elements, resistor , capacitor, interconnects, sheet resistance & standard unit capacitance concepts delay unit time, inverter delays , driving capacitive loads, propagate delays, MOS mask layer, stick diagram, design rules and layout, symbolic diagram, mask feints, scaling of MOS circuits.

**Unit-III** **10 hours**

**Basics of Digital CMOS Design:** Combinational MOS Logic circuits-Introduction, CMOS logic circuits with a MOS load, CMOS logic circuits, complex logic circuits, Transmission Gate. Sequential MOS logic Circuits - Introduction, Behavior of hi stable elements, SR latch Circuit, clocked latch and Flip Flop Circuits, CMOS D latch and triggered Flip Flop. Dynamic Logic Circuits - Introduction , principles of pass transistor circuits, Voltage boot strapping synchronous dynamic circuits techniques, Dynamic CMOS circuit techniques

**Unit-IV** **5 hours**

**CMOS Analog Design:** Introduction, Single Amplifier. Differential Amplifier, Current mirrors, Band gap references, basis of cross operational amplifier.

**Unit-V** **10 hours**

**Dynamic CMOS and Clocking**: Introduction, advantages of CMOS over NMOS, CMOS\SOS technology, CMOS\bulk technology, latch up in bulk CMOS., static CMOS design, Domino CMOS structure and design, Charge sharing, Clocking- clock generation, clock distribution, clocked storage elements

**TEXT BOOKS:**

1. Neil Weste and K. Eshragian, "**Principles of CMOS VLSI Design: A System Perspective**," 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.
2. Wayne, Wolf, "**Modern VLSI design: System on Silicon**" Pearson Education, Second Edition
3. Douglas A Pucknell & Kamran Eshragian , "**Basic VLSI Design**" PHI 3rd Edition (original Edition – 1994)
4. Sung Mo Kang & Yosuf Lederabic Law, "**CMOS Digital Integrated Circuits: Analysis and Design**", McGraw-Hill (Third Edition)

**EEC7208 ASIC DESIGN 3-0-0 Credits 3**

**Unit-I** **15 hours**

Introduction: Full Custom with ASIC, Semi custom ASICS, Standard Cell based ASIC, Gate array based ASIC, Channeled gate array, Channel less gate array, structured get array, Programmable logic device, FPGA design flow, ASIC cell libraries

Data Logic Cells: Data Path Elements, Adders, Multiplier, Arithmetic Operator, I/O cell, Cell Compilers

**Unit-I** **15 hours**

ASIC Library Design: Logical effort: practicing delay, logical area and logical efficiency logical paths, multi stage cells, optimum delay, optimum no. of stages, library cell design.

Low-Level Design Entry: Schematic Entry: Hierarchical design. The cell library, Names, Schematic, Icons & Symbols, Nets, schematic entry for ASIC'S, connections, vectored instances and buses, Edit in place attributes, Netlist, screener, Back annotation

Programmable ASIC: programmable ASIC logic cell, ASIC I/O cell

**Unit-III** **15 hours**

A Brief Introduction to Low Level Design Language: an introduction to EDIF, PLA Tools, an introduction to CFI designs representation. Half gate ASIC. Introduction to Synthesis and Simulation;

ASIC Construction Floor Planning and Placement And Routing: Physical Design, CAD Tools, System Partitioning, Estimating ASIC size, partitioning methods. Floor planning tools, I/O and power planning, clock planning, placement algorithms, iterative placement improvement, Time driven placement methods. Physical Design flow global Routing, Local Routing, Detail Routing, Special Routing, Circuit Extraction and DRC.

**Note All Designs Will Be Based On VHDL

TEXT BOOKS:

1. M.J.S .Smith, - "Application – Specific Integrated Circuits" – Pearson Education, 2003.
2. Jose E.France, Yannis Tsividis, "Design of Analog-Digital VLSI Circuits for Telecommunication and signal processing", Prentice Hall, 1994.

## EEC7209 LOW POWER VLSI DESIGN 3-0-0 Credits 3

**Unit-I** **12 hours**

Introduction : Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation

**Unit-II** **10 hours**

Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.

Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

**Unit-III** **18 hours**

Low Power Design Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library

Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network

**Unit-IV** **5 hours**

Algorithm & Architectural Level Methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

TEXT BOOKS:

1. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000
2. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002
3. Rabaey, Pedram, "Low Power Design Methodologies" Kluwer Academic, 1997

**EEC7210 DESIGN OF ANALOG & MIXED MODE VLSI CIRCUITS 3-0-0**
**Credits 3**

**Unit-I** **8 hours**

Introduction to CMOS Analog Circuits : MOS transistor DC and AC small signal parameters from large signal model,

**Unit-II** **15 hours**

Common Source Amplifier : with resistive load, diode load and current source load, Source follower, Common gate amplifier, Cascode amplifier, Folded Cascode, Frequency response of amplifiers, Current source/sink/mirror, Matching, Wilson current source and Regulated Cascode current source, Band gap reference,

**Unit-III** **15 hours**

Differential Amplifier, Gilbert cell, Op-Amp, Design of 2 stage Op-Amp, DC and AC response, Frequency compensation, slew rate, Offset effects, PSRR, Noise, Comparator,

**Unit-IV** **9 hours**

Sense Amplifier, Sample and Hold, Sampled data circuits, Switched capacitor filters, DAC, ADC, RF amplifier, Oscillator, PLL, Mixer.

TEXT BOOKS:


1. Razavi B., “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001
2. R. Jacob Baker,”CMOS: Mixed-Signal Circuit Dedsign”, John Wiley, 2008
3. Baker, Li, Boyce, “CMOS: Circuit Design, Layout and Simulation”, Prentice Hall of India, 2000
4. E. Allen, Douglas R. Holberg, “CMOS Analog circuit Design”

**EEC7211 ALGORITHMS FOR VLSI DESIGN 3-0-0 Credits 3**

**Unit-I** **8 hours**

Logic Synthesis & Verification: Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.

**Unit-II** **15 hours**

VLSI Automation Algorithms:
Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms

Placement, Floor Planning & Pin Assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment

**Unit-III** **15 hours**

Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches

Detailed Routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms

Over The Cell Routing & Via Minimization: two layers over the cell routers, constrained & unconstrained via minimization

**Unit-IV** **7 hours**

Compaction: problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction

TEXT BOOKS:

1. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.
2. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.
3. Rolf Drechsheler : "Evolutionary Algorithm for VLSI", Second edition
4. Trimburger, "Introduction to CAD for VLSI", Kluwer Academic publisher, 2002

**EEC7212 TESTING AND VERIFICATION OF VLSI CIRCUITS 3-0-0**
**Credits 3**

**Unit-I** **10 hours**

Introduction: Scope of testing and verification in VLSI design process; Issues in test and verification of complex chips; embedded cores and SOCs

**Unit-II** **10 hours**

Fundamentals of VLSI testing, Fault models. Automatic test pattern generation, Design for testability, Scan design, Test interface and boundary scan.

**Unit-III** **10 hours**

System Testing and test for SOCs, Iddq testing, Delay fault testing, BIST for testing of logic and memories, Test automation.

**Unit-IV** **15 hours**

Design Verification Techniques based on simulation, analytical and formal approaches, Functional verification, Timing verification, Formal verification, Basics of equivalence checking and model checking,

TEXT BOOKS :


1. M. Abramovici, M. A. Breuer, A. D. Friedman, “Digital Systems Testing and Testable Design” Piscataway, New Jersey: IEEE Press, 1994

2. M. Bushnell and V. D. Agarwal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000

3. T.Kropf, "Introduction to Formal Hardware Verification", Springer Verlag, 2000.

4. P. Rashinkar, Paterson and L. Singh, "System-on-a-Chip Verification-Methodology and Techniques", Kluwer Academic Publishers, 2001.

5.Samiha Mourad and Yervant Zorian, “Principles of Testing Electronic Systems”, Wiley (2000).

**EEC7213 Passive Microwave Devices & Circuits 3-0-0 Credits 3**

**Unit-I** **10 hours**

The transmission line section as a basic component; Application of Thevenin's theorem to a transmission line; Transfer function of a transmission line section; T and PI representation of a transmission line section;

**Unit-II** **10 hours**

Analysis of two ports and multiports network by using Z, Y and transmission matrix; S-parameter analysis of the microwave circuits; Conversion of Z, Y, transmission parameters and S-parameters;

**Unit-III** **15 hours**

Inter valley Scattering, Gunn diodes, IMPATT diodes.

Matching networks: Reactive matching network using the lumped elements; Quarter wavelength transformer, multi section transformer matching section; Lumped planar components like capacitor, inductor and balun; Power divider, Branch line coupler, hybrid ring coupler, directional coupler; Analysis of these components using the S-parameters; Richard transformation and Kurda identities; Inverters, Design of microwave planar filters;

**Unit-IV** **10 hours**

Planar Non reciprocal devices: Circulator, delay lines and phase shifters; MEMS technology based microwave components like switches, filters, phase shifters and delay lines.

**TEXT BOOKS:**


1.B. Bhat & S. Koul , Stripline – Loke transmission lines for MICS, John Wiley.
2. T.K.Ishii, Hand book of Microwave Technology , VOL .**I,** Academic press.
3. Y. Konishi, Microwave integrated circuit , Marcel Dekker.
4. S.Y. Liao , Microwave Circuit Analysis and Amplifier Design , PH.
5. B. Razavi , RF Micro – Electronics, PH.
6. M.I.Skolink – Introduction to Radar System, McGraw Hill
7. B.Edde- Radar, Principles, Technology,Application- Prentice Hall
8. D.K.Batras- Modern Radar Systems Analysis – Artech House

**EEC7214 ANTENNA THEORY & DESIGN 3-0-0 Credits 3**

**Unit-I** **12 hours**

**Antenna Fundamentals and Definitions**: Radiation mechanism - over view, Electromagnetic Fundamentals, Solution of Maxwell's Equations for Radiation Problems, Ideal Dipole, Radiation Patterns, Directivity and Gain, Antenna Impedance, Radiation Efficiency. Antenna Polarization

**Resonant Antennas:** Wires and Patches, Dipole ntennas, Yagi - Uda Antennas, Micro strip Antenna.

**Arrays:** Array factor for linear arrays, uniformly excited, equally spaced Linear arrays, pattern multiplication, directivity of linear arrays, non- uniformly excited - equally spaced linear arrays, Mutual coupling, multidimensional arrays, phased arrays, feeding techniques, perspective on arrays.

**Unit-II** **12 hours**

**Broad band Antennas**: Traveling - wave antennas, Helical antennas, Biconical antennas, sleave antennas, and Principles of frequency - independent Antennas, spiral antennas, and Log - Periodic Antennas.

**Aperture Antennas:** Techniques for evaluating Gain, reflector antennas - Parabolic reflector antenna principles, Axi -symmetric parabolic reflector antenna, offset parabolic reflectors, dual reflector antennas, Gain calculations for reflector antennas, feed antennas for reflectors, field representations, matching the feed to the reflector, general feed model, feed antennas used in practice.

**Unit-III** **12 hours**

**Antenna Synthesis:** Formulation of the synthesis problem, synthesis principles, line sources shaped beam synthesis, linear array shaped beam synthesis — Fourier Series, Woodward — Lawson sampling method, comparison of shaped beam synthesis methods, low side lobe narrow main beam synthesis methods Dolph Chebyshev linear array, Taylor line source method.

**Method of Moments :** Introduction to method of Moments, Pocklington's integral equation, integral equations and Kirchoff's Networking Equations, Source Modeling Weighted residuals formulations and computational consideration, calculation of antenna and scatter characteristics.

**Unit-IV** **10 hours**

**CEM for Antennas** : Finite Difference Time Domain Method Geometrical Optics Wedge diffraction theory, ray fixed coordinate system, uniform theory of wedge diffraction, E - Plane analysis of Horn antennas. Cylindrical parabolic antenna, radiation by a slot on a finite ground plane, radiation by a monopole on a finite ground plane, equivalent current concepts, multiple diffraction formulation, by curved surfaces, physical optics, method of stationary phase, physical theory of diffraction, cylindrical parabolic reflector antennas.

**TEXT BOOKS:**


1. Stutzman and Thiele, "**Antenna Theory and Design**", 2nd Ed, John Wiley and Sons Inc.
2. C. A. Balanis: "**Antenna Theory Analysis and Design"**, John Wiley, 2nd Edition, 1997
3. Kraus: "**Antennas"**, McGraw Hill, TMH, 3" Edition, 2003
4. Kraus and R.J. Marhefka: "**Antennas"**, McGraw Hil1, 2nd Edition, 1998

**EEC7215 OPTICAL COMMUNICATION & NETWORKING 3-0-0 Credits 3**

**Unit-I** **12 hours**

Introduction: Propagation of signals in optical fiber, different losses, nonlinear effects, solitons, optical sources, detectors.

Optical Components: Couplers, isolators, circulators, multiplexers, filters, gratings, interferometers, amplifiers.

**Unit-II** **8 hours**

Modulation — Demodulation: Formats, ideal receivers, Practical detection receivers, Optical preamplifier, Noise considerations, Bit error rates, Coherent detection.

**Unit-III** **15 hours**

Transmission System Engineering: system model, power penalty, Transmitter, Receiver, Different optical amplifiers, Dispersion.

Optical Networks: Client layers of optical layer, SONET/SDH, multiplexing, layers, frame structure, ATM functions, adaptation layers, Quality of service and flow control, ESCON, HIPPI.

WDM Network Elements: Optical line terminal optical line amplifiers, optical cross connectors, WDM network design, cost trade offs, LTD and RWA problems, Routing and wavelength assignment, wavelength conversion, statistical dimensioning model.

**Unit-IV** **10 hours**

Control and Management: network management functions, management frame work, Information model, management protocols, layers within optical layer performance and fault management, impact of transparency, BER measurement, optical trace, Alarm management, configuration management.

TEXT BOOKS:

1. John M. Senior, “Optical Fiber Communications”, Pearson edition, 2000.
2. Rajiv Ramswami, N Sivaranjan, “Optical Networks”, M. Kauffman Publishers, 2000.
3. Gerd Keiser, “Optical Fiber Communication”, MGH, 1 991.
4. G. P. Agarawal, “Fiber Optics Communication Systems”, John Wiley NewYork, 1997
5. P.E. Green, “Optical Networks”, Prentice Hall, 1994

**EEC7216 WIRELESS COMMUNICATIONS 3-0-0 Credits 3**

**Unit-I** **12 hours**

Radio Propagation: Free space propagation model, Relating power to electric field, reflection, ground reflection diffraction, scattering, practical link budget design using path loss models, outdoor propagation models, indoor propagation models, signal penetration into buildings, ray tracking and site specific modeling, small scale multi-path propagation, impulse response model of a multi-path channel, small scale multi-path measurements, parameters of mobile multi-path channels, types of small scale fading, Rayleigh and Ricean distributions, statistical models for multi-path fading channels.

**Unit-II** **8 hours**

Diversity Techniques: Concepts of Diversity branch and signal paths, Combining and switching methods, C/N, C/I performance improvements, Average Pe, performance improvement, RAKE receiver.

**Unit-III** **10 hours**

Cellular Concept: Frequency reuse, channel assignment strategies, handoff strategies; interference and system capacity, trunking and grade of service, improving coverage and capacity in cellular systems. FDMA, TDMA, spread spectrum multiple access, SDMA, packet Radio, capacity of cellular systems.

**Unit-IV** **5 hours**

Personal Mobile Satellite Communications: Integration of GEO, LEO, and MEO Satellite and Terrestrial mobile systems, personal satellite Communications programs.

**Unit-II** **10 hours**

CDMA Systems Implementation: Is-95 System Architecture, Soft Handoff and Power Control in IS-95 CDMA, cdma2000 System. Signal reception: Wireless signaling environment, basic receiver signal processing for wireless, blind multi-user detection, linear receivers for synchronous CDMA, blind multi-user detection direct methods, blind multi-user detection subspace methods, performance of blind multi-user detector, subspace tracking algorithms, blind multi-user detector in multi-path channels.

TEXT BOOKS:

1. Theodore S. Rappaport, “Wireless Communications: Principles and Practice,” 2nd edition, Prentice Hall of India, 2005.
2. Kamilo Feher, "Wireless Digital Communications: Modulation and Spread Spectrum Techniques,” Prentice Hall of India, 2004.
3. Vijay K. Garg, “IS-95 CDMA and cdma2000,” Pearson Education (Asia) Pte. Ltd, 2004.
4. Xiaodong Wang and Vincent Poor, “Wireless Communication Systems: Advanced Techniques for Signal Reception,” Pearson Education (Asia) Pte. Ltd, 2004

**EEC7217 ADVANCED DIGITAL COMMUNICATIONS 3-0-0 Credits 3**

**Unit-I** **8 hours**

**Digital Modulation Techniques:** QPSK, DPSK, FQPSK, QAM, M-QAM, OFDM, Optimum Receiver for Signals Corrupted by AWGN, Performance of the Optimum Receiver for Memory-less Modulation, Optimum Receiver for CPM Signals, Optimum Receiver for Signals with Random Phase in AWGN Channel.

**Unit-II** **8 hours**

**Coding Techniques:** Convolutional Codes, Hamming Distance Measures for Convolutional Codes; Various Good Codes, Maximum Likelihood Decoding of Convolutional codes, Error Probability with Maximum Likelihood Decoding of Convolutional Codes, Sequential Decoding and Feedback Decoding, Trellis Coding with Expanded Signal Sets for Band-limited Channels, Viterbi decoding.

**Unit-III** **8 hours**

**Communication through band limited linear filter channels:** Optimum receiver for channels with ISI and AWGN, Linear equalization, Decision-feedback equalization, reduced complexity ML detectors, Iterative equalization and decoding-Turbo equalization.

**Unit-IV** **8 hours**

**Adaptive Equalization:** Adaptive linear equalizer, adaptive decision feedback equalizer, adaptive equalization of Trellis- coded signals, Recursive least squares algorithms for adaptive equalization, self recovering (blind) equalization.

**Unit-IV** **15 hours**

**Spread Spectrum Signals for Digital Communication:** Model of Spread Spectrum Digital Communication System, Direct Sequence Spread Spectrum Signals, Frequency-Hopped Spread Spectrum Signals, CDMA, time-hopping SS, Synchronizatio of SS systems.

**Digital Communication Through Fading Multi-Path Channels:** Characterization of fading multi-path channels, the effect of signal characteristics on the choice of a channel model, frequency-Nonselective, slowly fading channel, diversity techniques for fading multi-path channels, Digital signal over a frequency-selective, slowly fading channel, coded wave forms for fading channels, multiple antenna systems.

**TEXT BOOKS:**


1. John G. Proakis, "**Digital Communications**", 4th edition, McGraw Hill, 2001.
2. Stephen G. Wilson, "**Digital Modulation and Coding**," Pearson Education (Asia) Pte. Ltd, 2003.
3. Kamilo Feher, "**Wireless Digital Communications: Modulation and Spread Spectrum Applications**," Prentice-Hall of India, 2004.
4. Andrew J. Viterbi, "**CDMA: Principles of Spread Spectrum Communications,"** Prentice Hall, USA, 1995

**EEC7218 RF AND MICROWAVE CIRCUIT DESIGN 3-0-0 Credits 3**

**Unit-I** **10 hours**

**Wave Propagation in Networks:** Introduction to RF/Microwave Concepts and applications; RF Electronics Concepts; Fundamental Concepts in Wave Propagation; Circuit Representations of two port RF/MW networks

**Unit-II** **10 hours**

**Passive Circuit Design:** The Smith Chart, Application of the Smith Chart in Distributed and lumped element circuit applications, Design of Matching networks.

**Unit-I** **10 hours**

**Basic Considerations in Active Networks:** Stability Consideration in Active networks, Gain Considerations in Amplifiers, Noise Considerations in Active Networks.

**Unit-I** **15 hours**

**Active Networks:** Linear and Nonlinear Design: RF/MW Amplifiers Small Signal Design, Large Signal Design, RF/MW Oscillator Design, RF/MW Frequency Conversion Rectifier and Detector Design, Mixer Design, RF/MW Control Circuit Design, RF/MW Integrated circuit design.

**TEXT BOOKS:**


1. Matthew M. Radmanesh**,** "**Radio Frequency and Microwave Electronics Illustrated"**, Pearson Education (Asia) Pte. Ltd., 2004.
2. Reinhold Ludwig and Pavel Bretchko, "**RF Circuit Design: "Theory and Applications**", Pearson Education (Asia) Pte. Ltd., 2004.
3. Malcolm R.Haskard; Lan. C. May, "Analog VLSI Design - NMOS and CMOS", Prentice Hall, 1998.
4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing", McGraw Hill, 1994.

**EEC7219 CMOS RF CIRCUIT DESIGN 3-0-0 Credits 3**

**Unit-I** **10 hours**

Introduction to RF Design and Wireless Technology: Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Intersymbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion

**Unit-II** **10 hours**

RF Modulation: Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures, Direct conversion and two-step transmitters

RF Testing: RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.

**Unit-III** **10 hours**

BJT and MOSFET Behavior at RF Frequencies: BJT and MOSFET behavior at RF frequencies, modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation

**Unit-IV** **15 hours**

RF Circuits Design: Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Various mixers- working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.

TEXT BOOKS:

1. B. Razavi, “RF Microelectronics” PHI 1998
2. R. Jacob Baker, H.W. Li, D.E. Boyce “CMOS Circuit Design, layout and Simulation”, PHI 1998.
3. Thomas H. Lee “Design of CMOS RF Integrated Circuits” Cambridge University press 1998.
4. Y.P. Tsividis, “Mixed Analog and Digital Devices and Technology”, TMH 1996

**EEC7220 MODELING AND SIMULATION OF NETWORKS 3-0-0 Credits 3**

**Unit-I** **10 hours**

Delay Models in Data Networks: Queuing Models, M/M/1, M/M/m, M/M/¥, M/M/m/m and other Markov System, M/G/1 System, Networks of Transmission Lines, Time Reversibility, Networks of Queues.

**Unit-I** **10 hours**

Multi-access Communication: Slotted Multi-access and the Aloha System, Splitting Algorithms, Carrier Sensing, Multi-access Reservations, Packet Radio Networks.

**Unit-III** **15 hours**

Routing in Data Networks: Introduction, Network Algorithms and Shortest Path Routing, Broadcasting Routing Information: Coping with Link Failures, Flow models, Optimal Routing, and Topological Design, Characterization of Optimal Routing, Feasible Direction Methods for Optimal Routing, Projection Methods for Optimum Routing, Routing in the Codex Network.

**Unit-IV** **10 hours**

Flow Control: Introduction, Window Flow Control, Rate Control Schemes, Overview of Flow Control in Practice, Rate Adjustment Algorithms.

TEXT BOOKS:

1. Dimitri Bertsekas and Robert Gallager, “Data Networks," 2nd edition, Prentice Hall of India, 2003.
2. William Stallings, “High-Speed Networks and Internets,” Pearson Education (Asia) Pte. Ltd, 2004.
3. J. Walrand and P. Varaya, “High Performance Communication Networks,” 2nd edition, Harcourt India Pte. Ltd. & Morgan Kaufman, 2000.